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FPGA Implementation
of LTE Downlink

Transceiver with

Synchronization and

Equalization Sara M.

Hassan Modern

Academy, Cairo, Egypt

Abdelhalim Zekry Ain

Shams University,

Cairo, Egypt ABSTRACT

Long Term Evolution

(LTE) is an advanced

standard of the mobile

communication

systems. LTE has been

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developed by

FPGA

Implementation of LTE Downlink Transceiver with ...

This paper presents the design and implementation of the LTE-A downlink transmitter and receiver using a Field Programmable Gate Array (FPGA) according to release 10/11 on Virtex 6 XC6VLX240T FPGA.

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(PDF) FPGA Transceiver With Implementation of LTE-Advanced Downlink ...

This paper presents a Field Programmable Gate Array (FPGA) design and implementation of the LTE downlink transmitter and receiver according to releases 8 and 9 on Virtex 6 XC6VLX240T FPGA kit using Xilinx® ISE® Design Suite

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FPGA architecture for the implementation of LTE downlink control channels in enviroMIMO nment. A brief out line of LTE downlink Control Channels is given in

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section 2; system model and its processing steps are explained in section the concept of 3; Alamouti's Space Frequency Block Codes is explained

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Abstract: Hardware implementation of LTE-Advanced systems using FPGA and ASIC technology is a highly promising technology. This article proposed a reliable and effective architecture for a LTE downlink transmitter under different antenna configurations including SISO 1×1; MIMO 2×2.

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FPGA and ASIC With implementation of reliable and effective ...

Fpga Implementation
Of Lte Downlink LTE
Release 8 can provide
up to 50 Mbps for
uplink and. 100 Mbps
for downlink, while LTE-
A, starting from
Release 10, can
provide up to 1 Gbps
as peak data rates for
downlink, as well as.
higher throughput,

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higher coverage, and lower latencies [1-9].

Fpga Implementation Of Lte Downlink Transceiver With

In thesis a Digital Down Converter (DDC) for Long Term Evolution (LTE) signals is designed. The DDC shall be implemented in hardware in a Field Programmable Gate Array (FPGA). For an FPGA the desired

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operating speed is high. The purpose of this thesis is therefore to determine if it is possible to design such a system.

Implementation of a DDC for LTE in a FPGA

implementation. Hence, the system architecture should be well designed to achieve high data rate and good error-rate performance. This

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paper presents an architecture and an FPGA prototype of an LTE uplink MIMO receiver. This work, to the best of the author's knowledge, is the first FPGA prototype of the LTE

FPGA Prototyping of A High Data Rate LTE Uplink Baseband

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Hardware
implementation of LTE-
advanced systems

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using FPGA technology
is a highly promising
technology for mobile
communications and
wireless networks
researchers. The
objective of this paper
is to improve the
processing speed; the
system capabilities;
the power
consumption, and the
processing delay of LTE-
advanced downlink
control channels due to
the parallel processing
nature of FPGA.

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Fast Implementation of Different LTE Physical Downlink ...

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implementation of lte
downlink This paper
presents the design
and implementation of
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transmitter and
receiver using a Field
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Here's a review of the
LTE algorithms and a
practical
implementation on a
Xilinx FPGA. The
reference design is
tested using multiple
video stream with

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varying encoding rates.

By Rob Payne, Xilinx

dspdesignline.com

(February 06, 2009)

The next generation of
the 3GPP

Implementing LTE on FPGAs - Design And Reuse

Hardware

implementation of LTE-

advanced systems

using FPGA technology

is a highly promising

technology for mobile

communications and

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wireless network
researchers. The
objective of this paper
is to improve the
processing speed; the
system

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A sinusoid modulated
onto a 32 MHz IF
carrier. An LTE
downlink signal with a
bandwidth of 1.4 MHz,
modulated onto a 32
MHz IF carrier. The
example measures

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signal quality at the output of the floating-point and fixed-point DDCs, and compares the two. Finally, FPGA implementation results are presented.

HDL Implementation of a Digital Down-Converter for LTE ...

Fpga Implementation Of An Lte This paper presents the simulation and the FPGA implementation of the LTE downlink physical

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layer (on Virtex 6
XC6VLX240T FPGA kit)
according to release 9
using Xilinx package
version 12.1.

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Array (FPGA) design
and implementation of
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Terms SDR, LTE, 4G,
3GPP, OFDM,
Transmitter , 2G ,3G,
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layer, release 8,
release 9 Xilinx Design

Software Defined Radio Implementation of LTE Transmitter

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