

Turbo Coding Hardware Acceleration Of An Egprs 2 Turbo Decoder On An Fpga

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Turbo Coding Hardware Acceleration Of codes. In order to study the use of hardware acceleration for turbo code per-formance simulations, a simulator set-up has to be implemented for the specific system. One key factor needed for this type of simulator set-up to study the perfor-mance of the error-correcting codes is the simulation of random noise. In this

Turbo Code Performance Analysis using Hardware Acceleration
This report documents the work for the master thesis: Turbo Coding - Hardware Acceleration of an EGPRS-2 Turbo Decoder on an FPGA. It represents the work done on a semester long project at Applied Signal Processing and Implementation master specialization at Department of Electronic Systems, Aalborg University, Denmark.

Hardware Acceleration of an EGPRS-2 Turbo Decoder on an FPGA
The simulations needed to obtain such results are very time consuming and this poses achallenge to studying the problem. This thesis investigates the use of hardware acceleration for performing fast simulations of turbo code performance.

Turbo Code Performance Analysis Using Hardware Acceleration
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GPU Code Acceleration. To speed up your code while prototyping, Communications Toolbox includes some features that can execute on a Graphics Processing Unit (GPU). You can use the gpuArray (Parallel Computing Toolbox) function to transfer data to the GPU and then call the gather (Parallel Computing Toolbox) function to retrieve the output data from the GPU.

Code Generation and Acceleration Support - MATLAB & Simulink
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